CLAIMS

What is claimed is

1. A method comprising:
fabricating a plurality of lands on a surface of a substrate; and
forming an off-center via in each land.

2. The method recited in claim 1, wherein each land has a geometric center and an edge, wherein each via has a geometric center, and wherein each via is formed with its geometric center in a region between the geometric center and the edge of a land.

3. The method recited in claim 2, wherein the geometric centers of vias of adjacent lands are offset in substantially the same direction.

4. The method recited in claim 2, wherein in the forming operation the vias are formed by drilling, and wherein the vias are drilled in a region between the geometric center and the edge of a land.

5. The method recited in claim 4, wherein no via is drilled at the geometric center of a land

6. The method recited in claim 4, wherein vias of adjacent lands are drilled at substantially the same distance from the geometric centers of the respective lands, and wherein the offsets of such vias from the geometric centers of the respective lands have substantially the same angle.

7. A method comprising:

fabricating a plurality of lands on a surface of a substrate;

forming an off-center via in each land;

applying a material over the surface of the substrate, including the vias, the material comprising a thermally expansive substance;

aligning an integrated circuit package having contacts comprising electrically conductive material with respect to the lands; and

heating the electrically conductive material and the lands until they join.

8. The method recited in claim 7, wherein the contacts form a portion of a ball grid array.

9. The method recited in claim 7, wherein the material comprises a volatile organic compound.

10. The method recited in claim 7, wherein the material is from the group comprising a solder mask, a solder flux, a solder paste, a solvent, and a via cap.

11. The method recited in claim 7, wherein the electrically conductive material comprises solder.

12. The method recited in claim 7, wherein the contacts are solder balls.

13. The method recited in claim 7, wherein each land has a geometric center and an edge, wherein each via has a geometric center, and wherein each via is formed with its geometric center in a region between the geometric center and the edge of a land.

14. The method recited in claim 13, wherein the geometric centers of vias of adjacent lands are offset in substantially the same direction.

15. The method recited in claim 13, wherein in the forming operation the vias are formed by drilling, wherein each land has an edge, and wherein the vias are drilled in a region between the geometric center and the edge of a land.

16. The method recited in claim 15, wherein no via is drilled at the geometric center of a land.

17. The method recited in claim 7, wherein in the applying operation the thermally expansive substance is applied to the interiors of two adjacent vias, and wherein in the heating operation the thermally expansive substance residing in the two adjacent vias is inhibited from causing the associated contacts to be bridged when the lands and contacts are subjected to heat.

18. A substrate comprising a plurality of lands, each land having a geometric center, wherein each land has a via therein that is offset with respect to the geometric center of the land.

19. The substrate recited in claim 18, wherein each land has an edge, wherein each via has a geometric center, and wherein the geometric center of each via is in a region between the geometric center and the edge of its associated land.

20. The substrate recited in claim 19, wherein the geometric centers of vias of adjacent lands are offset in substantially the same direction.

21. An electronic assembly comprising:

an integrated circuit package; and

a substrate having a plurality of lands, each land having an offset via, and each land being aligned with respect to a contact of the integrated circuit package.

22. The electronic assembly recited in claim 21, wherein each via inhibits a thermally expansive substance residing in the vias from causing adjacent contacts of the integrated circuit package to be bridged when the lands and contacts are subjected to heat.

23. The electronic assembly recited in claim 22, wherein the thermally expansive substance comprises a volatile organic compound.

24. The electronic assembly recited in claim 22, wherein the thermally expansive substance comprises a volatile liquid that forms a portion of a material from the group consisting of a solder mask, a solder flux, a solder paste, a solvent, and a via cap.

25. The electronic assembly recited in claim 21, wherein the lands comprise a first group having vias offset in a first direction, and a second group having vias offset in a second direction.

26. The electronic assembly recited in claim 21, wherein each land has a geometric center and an edge, wherein each via has a geometric center, and wherein each via is formed with its geometric center in a region between the geometric center and the edge of a land.

27. The electronic assembly recited in claim 26, wherein the geometric centers of vias of adjacent lands are offset from the geometric centers of such lands in the same direction.

28. An electronic system comprising an electronic assembly having an integrated circuit package, and a substrate having a plurality of lands, each land being aligned with respect to a respective contact of the integrated circuit package and comprising an offset via.

29. The electronic system recited in claim 28, wherein each land has a geometric center and an edge, wherein each via has a geometric center, and wherein the geometric center of each via is in a region between the geometric center and the edge of a land.

30. The electronic system recited in claim 29, wherein the geometric centers of vias of adjacent lands are offset from the geometric centers of such lands in the same direction.